REMARKS:

In the outstanding Office Action, the Examiner rejected claims 11-30. Claims 11, 15, 19, 23 and 27 are amended herein. Claims 13, 17, 21, 26 and 28-30 are cancelled herein without prejudice and claims 1-10 remain cancelled. No new matter is presented.

Proper support for the amendments can be found at least at page 33, line 6 through page 34, line 9; page 35, line 4 through page 37, line 11, FIG. 1 and corresponding text of the present application.

Thus, claims 11, 12, 14-16, 18-20, 22, 23-25 and 27 are pending and under consideration. The rejections are traversed below.

REJECTION UNDER 35 U.S.C. §102(e):

Claims 28, 29 and 30 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,049,860 (Krygowski). As mentioned above, claims 28-30 are cancelled herein.

Therefore, withdrawal of the rejection is respectfully requested.

REJECTION UNDER 35 U.S.C. §103(a):

Claims 11-27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Krygowski and Texas Instrument's Semiconductor Service Support (TI). As mentioned above, claims 13, 17, 21 and 26 are cancelled herein.

In Krygowski, multiplication, addition, normalization, and rounding are performed in computation stages (see, col. 4 lines 3-7). That is, Krygowski fails to teach or suggest "a first instruction decoding unit that decodes all other instructions with the exception of the first instruction into a second control signal as a through instruction", and "a first processing unit configured to perform a first operation on a first data when receiving the first control signal, and to pass through the first data when receiving the second control signal" (see detailed discussion of independent claims below).

The Examiner maintains the comparison of the Krygowski system that holds instruction data for each of the four pipeline stages in corresponding registers with the present invention. However, the Krygowski system requires staging registers at each stage of the pipeline for storing the types of instruction data (elements 20, 22, 25, 29 in FIG. 2). For example, when it is determined that there is data dependency between instructions, the store instruction is held in

the data input register (20) of the pipeline (see, col. 4, lines 35-52). That is, Krygowski requires that holding units be provided for each instruction data at each of the four pipeline stages.

The present invention reduces the number of latch circuits needed between processing stages for holding data in a pipeline operation. For example, as illustrated in FIG. 1, a decoder (3201) decodes all other instructions with the exception of the first instruction into a through instruction and causes only the first instruction to be processed in the first processing stage (see also, page 35, line 11-18). As further illustrated in FIG. 1, the second instruction and the processing result of the first instruction are held in the stage latch circuit (1102) (see also, FIG. 2 and corresponding text).

In contrast to Krygowski and TI, the present invention eliminates the need to provide a latch circuit for holding each kind of instruction passed between the processing stages of a pipeline operation.

Independent claim 11 recites, "a first instruction decoding unit that determines a kind of instruction in a current processing stage, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal as a through instruction upon determining at least the kind of instruction." Claim 11 also recites, "a first processing unit" and "a second processing unit" in "the current processing stage" and "a next processing stage", respectively, where "a latch circuit [is] provided between the current processing stage and a next processing stage" and holds "one of a result of the first operation and the first data passing through the first processing unit as a second data."

In addition, independent claim 11 recites, "a multiplexer provided in the next processing stage for selecting an output of the second processing unit or the second data held in the latch circuit based on an output of the second instruction decoding unit." Independent claims 19 and 27 recite similar features.

Independent claim 15 recites, "a first latch circuit provided in a current processing stage for storing a first data", "a bypass line provided in parallel with the first processing unit" and "a second latch circuit provided between the current processing stage and a next processing stage", where the second latch circuit holds "one of a result of the first operation and the first data bypassing the first processing unit through the bypass line as a second data." Claim 15 also recites, "a multiplexer in the current processing stage for selecting one of an output of the first processing unit or the first data held in the first latch circuit based on an output of the first instruction decoding unit." Independent claim 23 also recites similar features.

Krygowski and TI, alone or in combination, do not teach or suggest the above-discussed features of the independent claims.

It is submitted that the independent claims are patentable over the combination of Krygowski and TI.

For at least the above-mentioned reasons, claims depending from the independent claims are patentably distinguishable over the combination Krygowski and TI. The dependent claims are also independently patentable. For example, claim 12 recites that "the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal" (see also, claims 16, 20 and 24). The combination of the Krygowski and TI does not teach or suggest these features recited in dependent claims 12, 16, 20 and 24.

Therefore, withdrawal of the rejection is respectfully requested.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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